ECEC-355

Project 2: Single-cycle RISC-V Simulation

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1 Introduction

This project is intended to be a comprehensive introduction to single-cycle RISC-V simulation. You may work on this project in a team of up to three members.

2 Required Reading

Chapter 4. The Processor, Sections 4.1 – 4.4.

3 Development Environment

- Operating System: Linux.
- Code-base: `https://github.com/arghavanmh-drexel/DREXEL_DISCO_RISCV_projects.git`. Please *git clone* the repository to your Linux machine:

```
$ git clone https://github.com/arghavanmh-drexel/DREXEL_DISCO_RISCV_projects.git
```

4 Framework Overview

1. You will be working under directory *DREXEL_DISCO_RISCV_projects/project_2_3_4_5*. To navigate to the directory:

```
$ cd DREXEL_DISCO_RISCV_projects/project_2_3_4_5
```

2. To compile and run the simulator:

```
$ make
$ ./RVSim ../cpu_traces/project_two
```

5 Review of Byte-addressable Data Memory

1. Assume we have a size-of-24-bytes data memory as shown in Figure 1. How does int arr[3] = {19088743, 2882400001, 169552957} get stored (assume arr[0] points to 0th location) **Hints: Endianness**. Report the following in your report.

   (a) How much space (in byte) does one integer occupy considering a RISC-V architecture?

   (b) Draw the data mapping.

   ****p.s - consider long ints when storing the array****

2. Continuing with 1, what is the value of x10 (assume x23 = 0)?

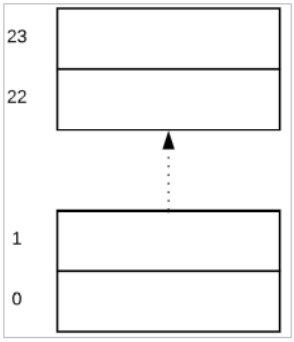

Figure 1: Endianness

```
ld x8, 0(x23)
ld x9, 16(x23)
add x10, x8, x9
```

6 Extending the Framework

Extend *Core.{h,c}* to simulate the behavior of a single-cycle RISC-V CPU as shown in Figure 2. Test your simulator using *../cpu_traces/project_two* with the following configurations. Report the final values of all registers and memory locations in *../cpu_traces/project_two*.

1. Set x8 to 16;
2. Set x10 to 4;
3. Set x11 to 0;
4. Set x22 to 1;
5. Set x24 to 0;
6. Set x25 to 4;
7. Set data memory from 0th location to uint64_t arr[] = {16, 128, 8, 4}

7 Submission

Your submission file should in a zip format including the following items. Please use "firstname-lastname-project2.zip" for the name of your submission file and submit it to BBlearn.

1. Summary of your experiments in Section 4 and 5. Compile your report in PDF format.
2. All the source codes.
3. Zip above and submit through Bblearn.

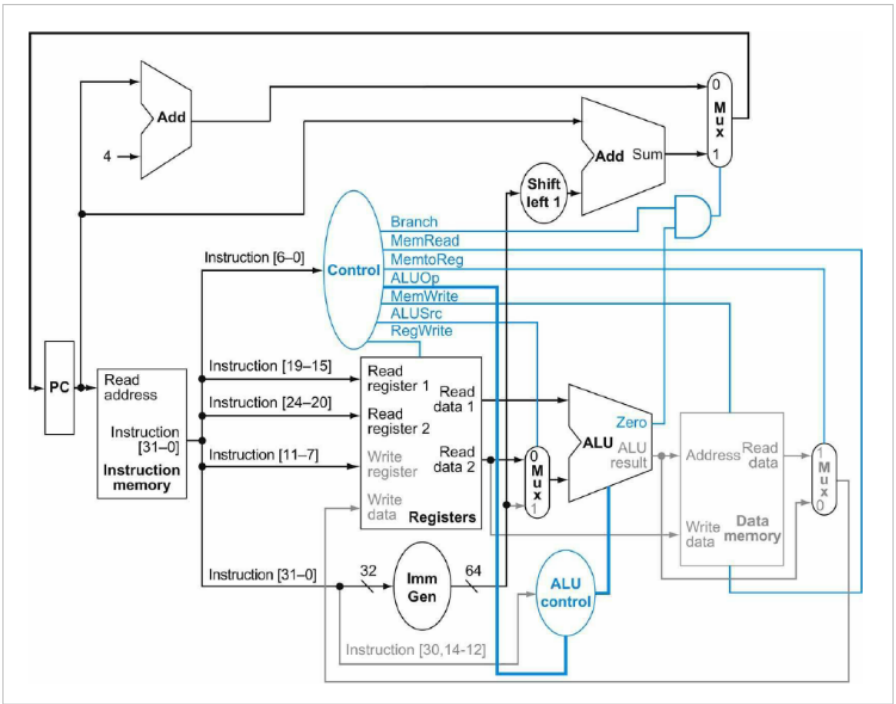

Figure 2: A Single-cycle RISC-V CPU